OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
JC113

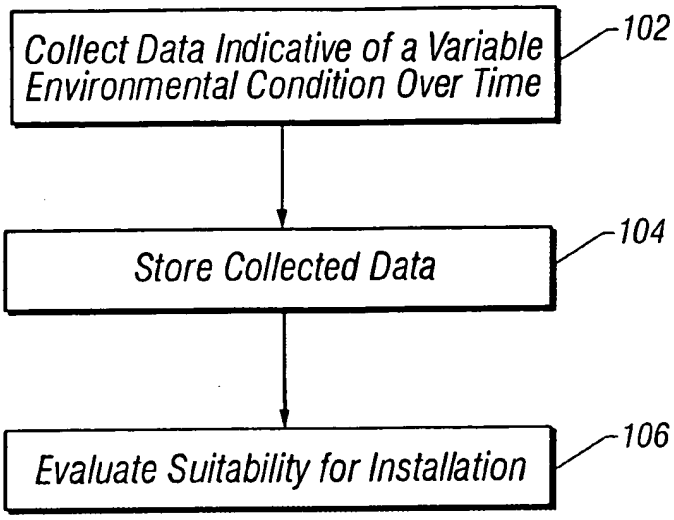

FIG. 1

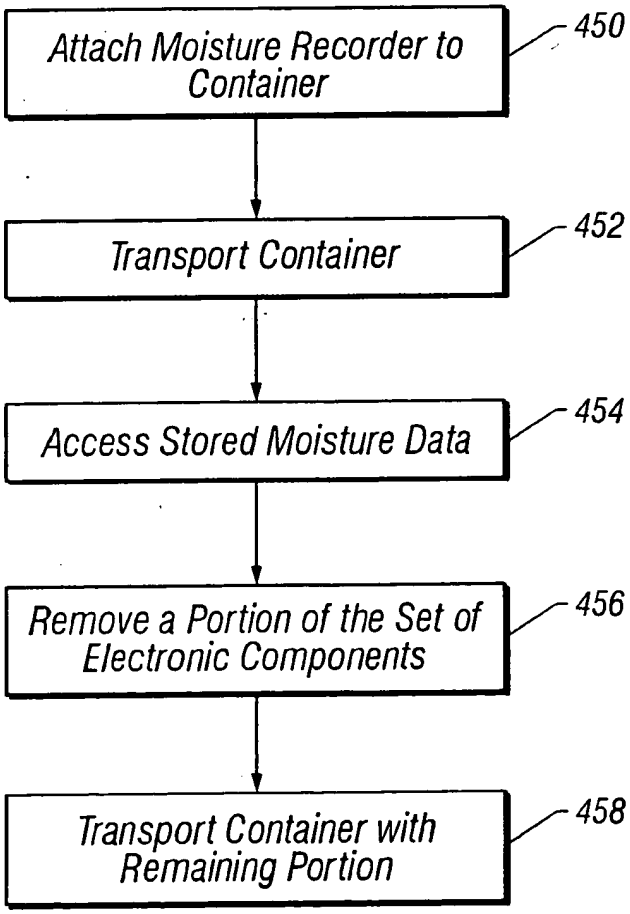

FIG. 4

OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
TC 1713

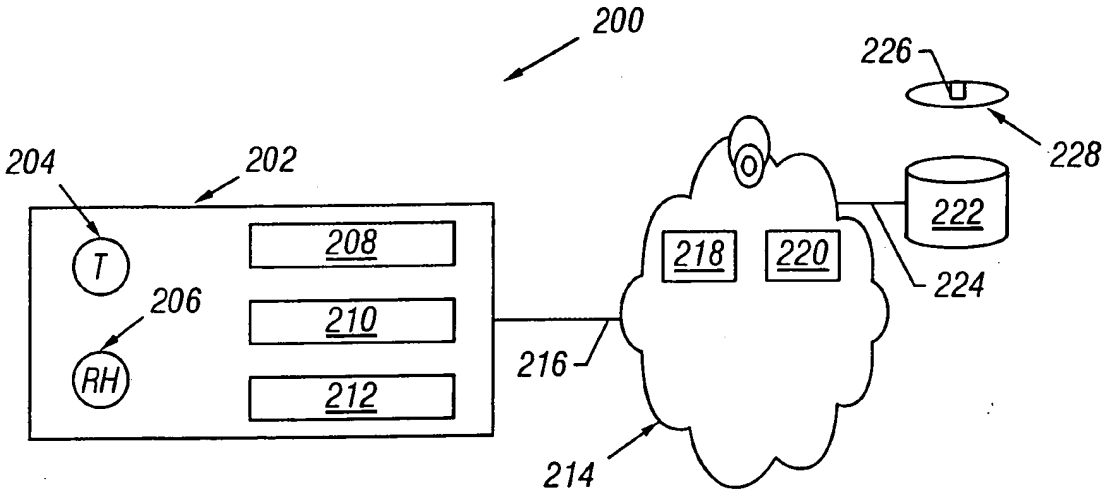

FIG. 2A

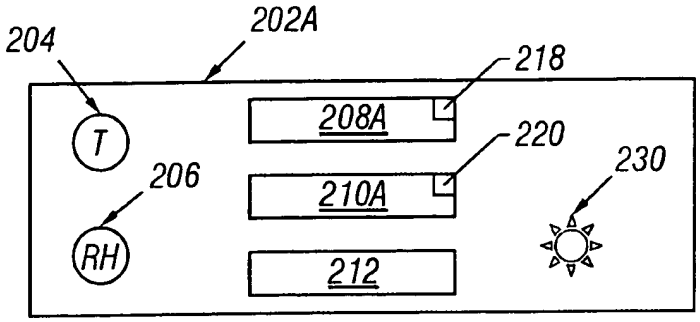

FIG. 2B

OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
JC113

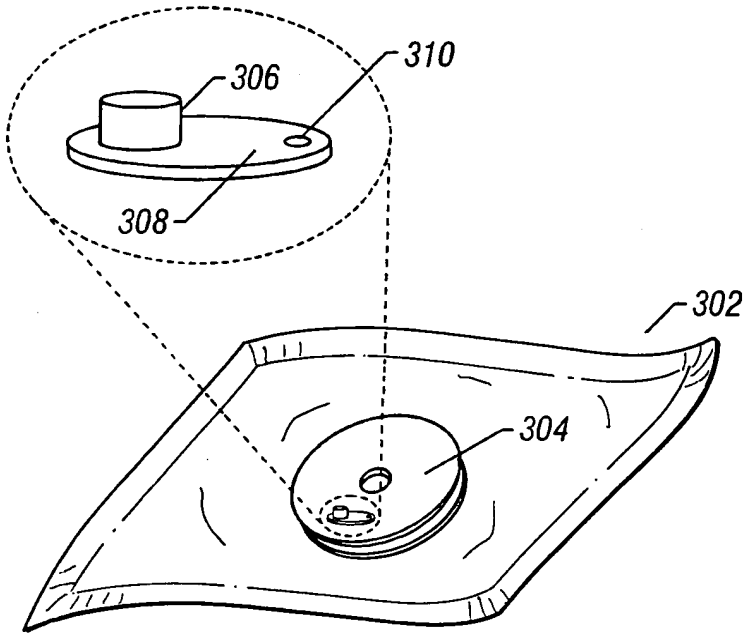

FIG. 3A

OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
JC113

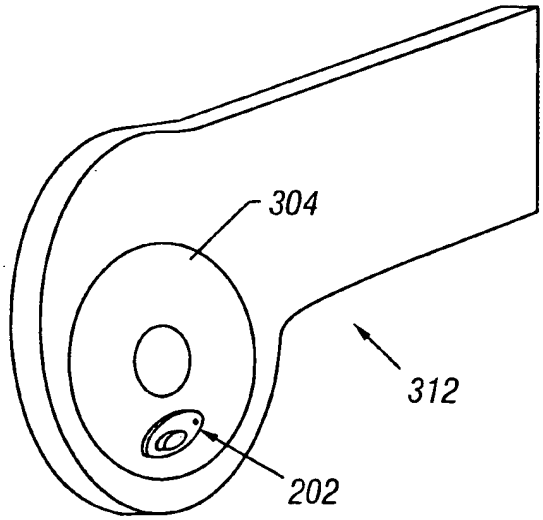

FIG. 3B

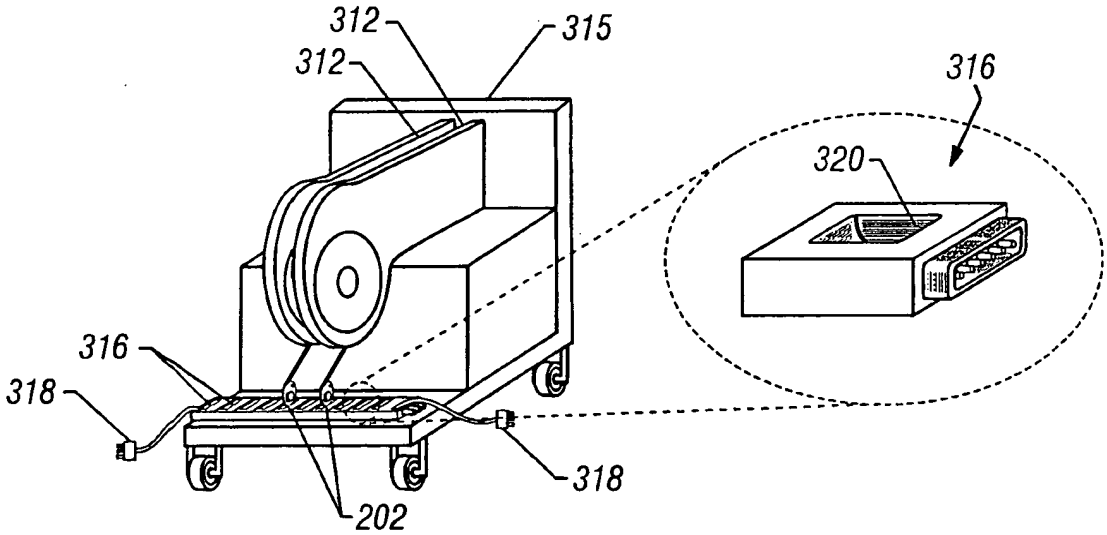

FIG. 3C

OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
TC1100

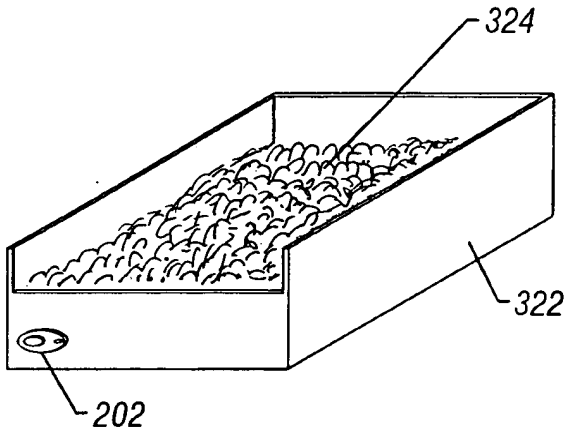

FIG. 3D

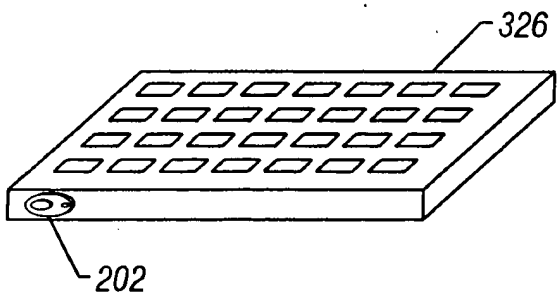

FIG. 3E

OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
JC113

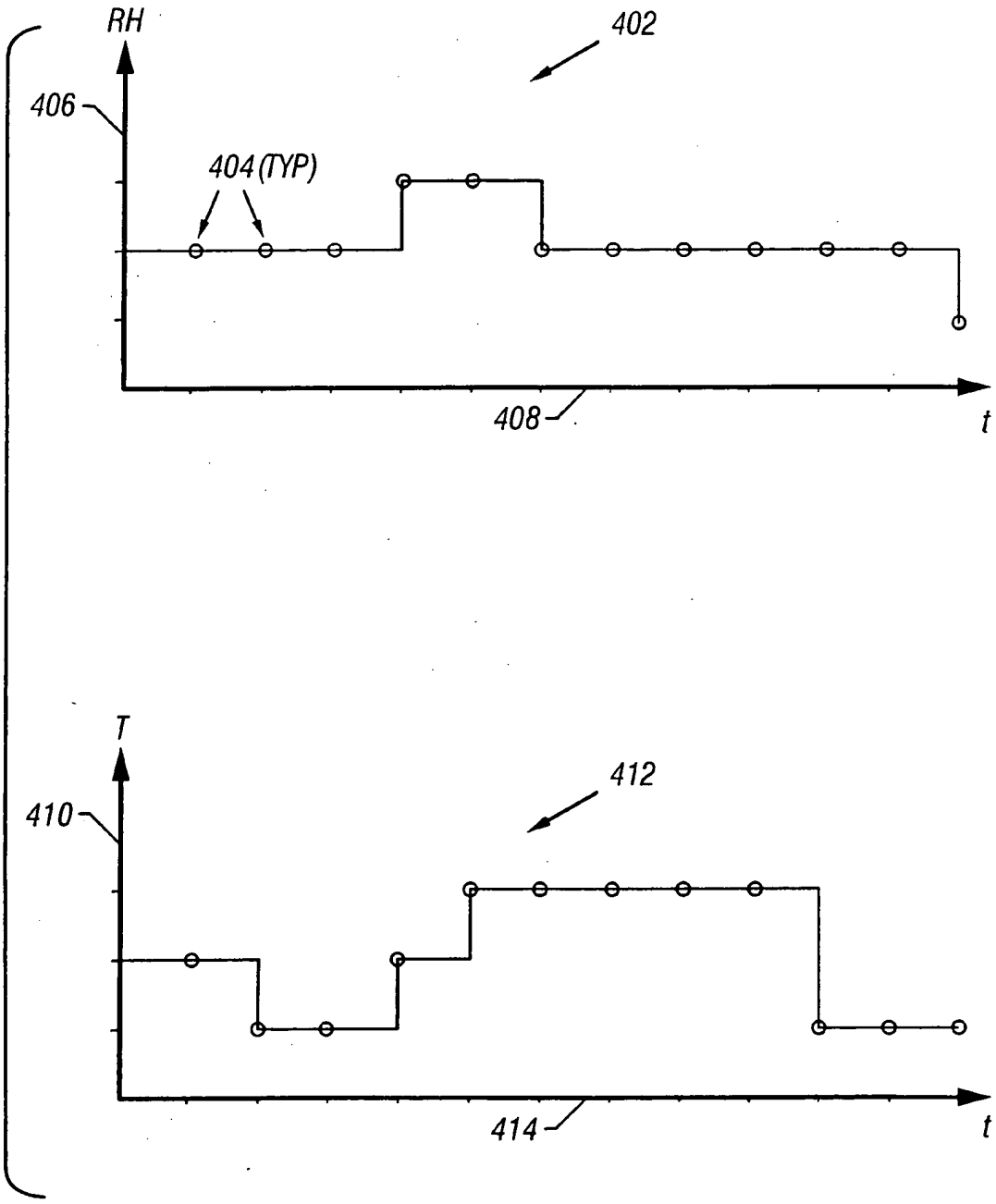

FIG. 5

OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
JC13

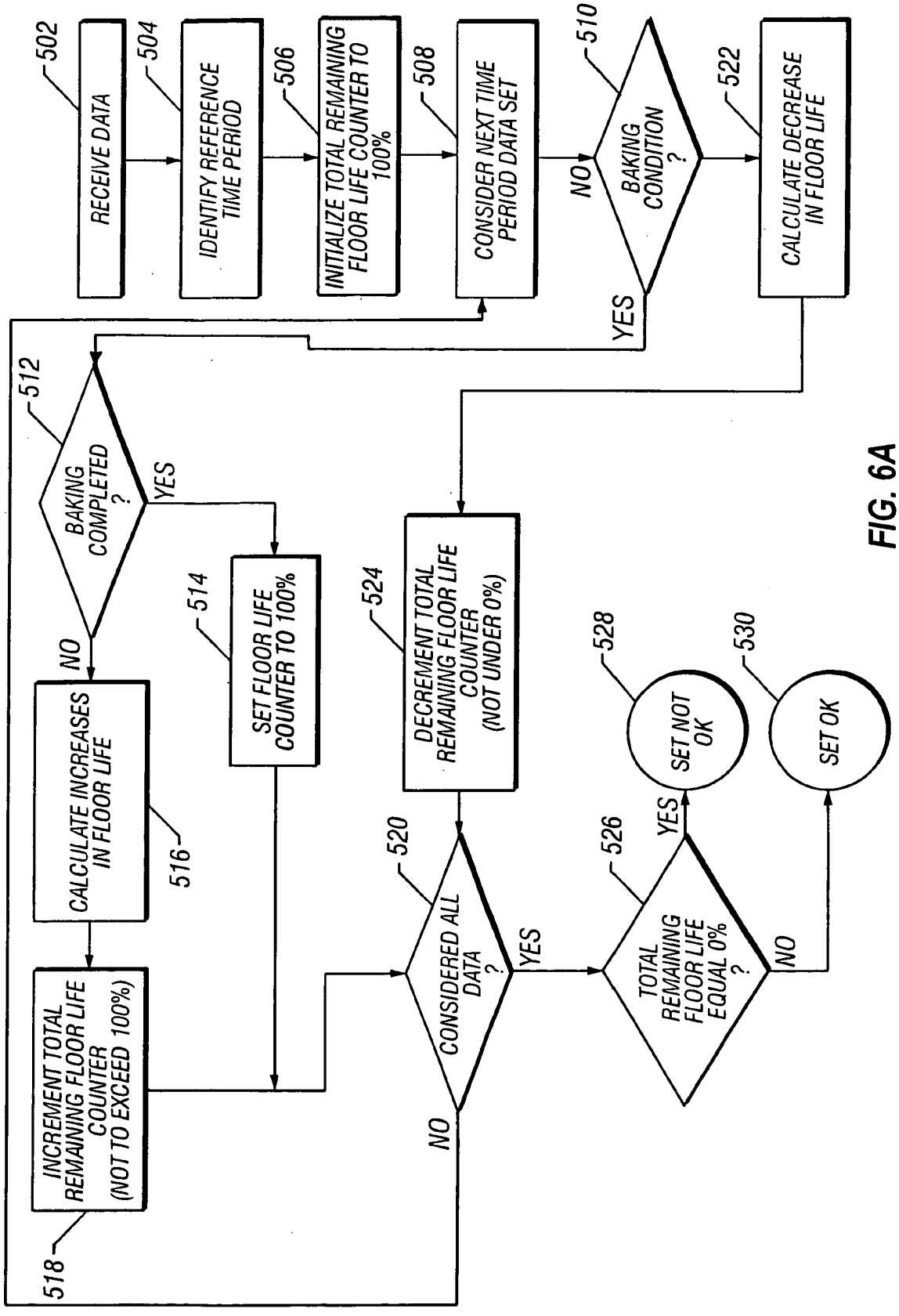

FIG. 6A

OIPE JC113 MAY 19 2004 PATENT & TRADEMARK OFFICE

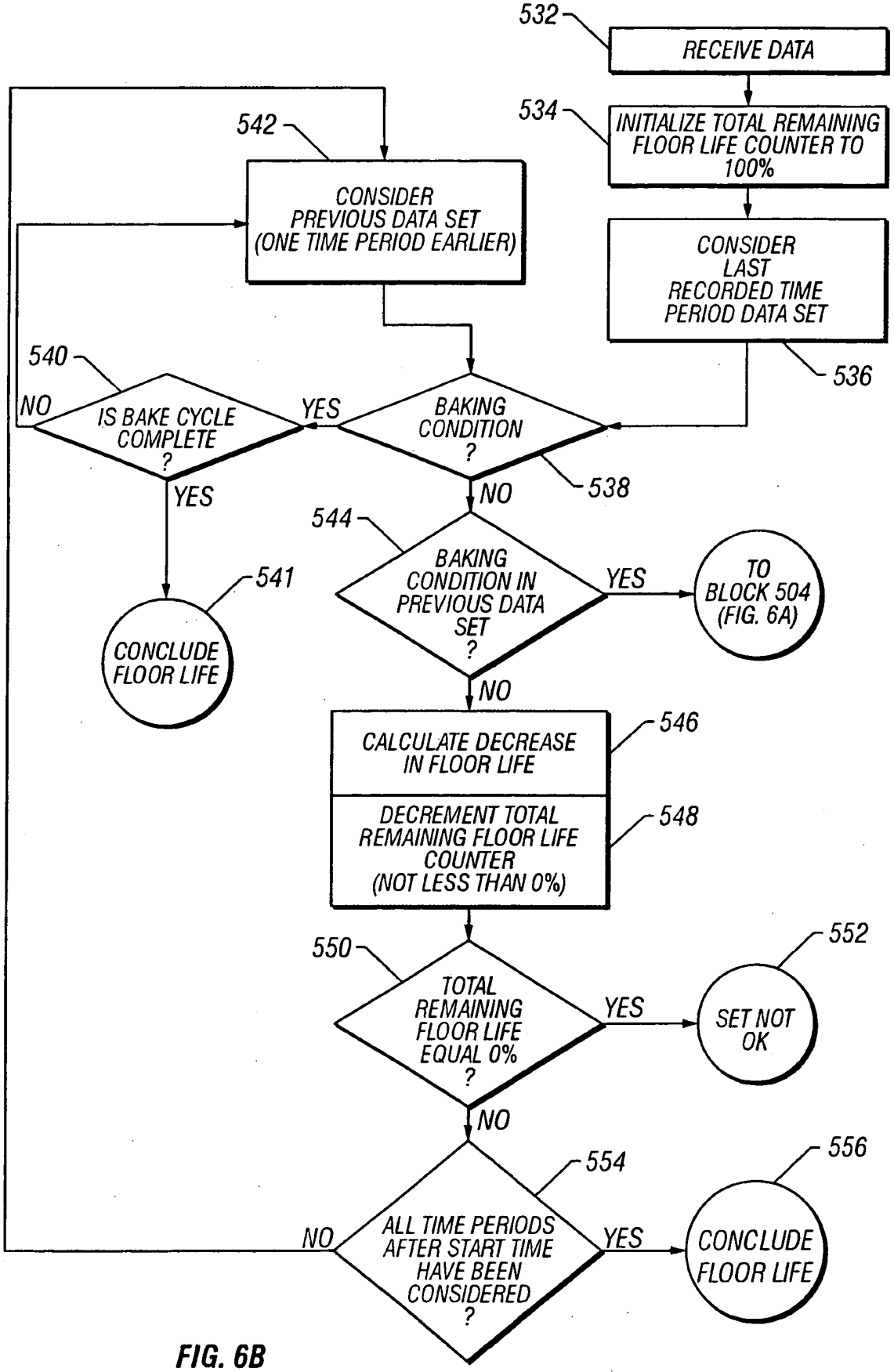

FIG. 6B

OIPE JC113 MAY 19 2004 PATENT & TRADEMARK OFFICE

602

IPC/JEDEC J-STD-033 April 1999

TABLE 5 Recommended Equivalent Total Floor Life (days) @ 20°C,25°C & 30°C
For ICs with Novolac, Biphenyl and Multifunctional Epoxies
(Reflow at same temperature at which the component was classified)

		Maximum Percent Relative Humidity								604
Body Thickness (t)	M.S.Level	20%	30%	40%	50%	60%	70%	80%	90%	
t≥3.1mm PQFPs>84 pins. PLCCs (square) MQFPs or PBGAs	Level 2a	∞ ∞ ∞	60 78 103	41 53 69	33 42 57	28 36 47	10 14 19	7 10 13	6 8 10	30°C 25°C 20°C
	Level 3	10 13 17	9 11 14	8 10 13	7 9 12	7 9 12	5 7 10	4 6 8	4 5 7	30°C 25°C 20°C
	Level 4	4 5 7	4 5 7	4 5 7	3 5 7	3 4 6	3 3 5	2 3 4	2 3 4	30°C 25°C 20°C
	Level 5	3 5 7	3 4 6	2 4 5	2 3 5	2 3 4	2 2 3	1 2 3	1 2 3	30°C 25°C 20°C
	Level 5a	1 2 4	1 2 3	1 2 3	1 2 3	1 2 2	1 1 2	1 1 2	1 1 2	30°C 25°C 20°C
t≤2.1mm t<3.1mm PLCCs(rectangular)18-32 pins SOICs(wide body) SOICs≥20pins PQFPs≤80pins	Level 2a	∞ ∞ ∞	∞ ∞ ∞	86 148 ∞	39 51 69	28 37 49	4 6 8	3 4 5	2 3 4	30°C 25°C 20°C
	Level 3	19 25 32	12 15 19	9 12 15	8 10 13	7 9 12	3 5 7	2 3 5	2 3 4	30°C 25°C 20°C
	Level 4	5 7 9	4 5 7	4 5 6	3 4 6	3 4 5	2 3 4	2 2 3	1 2 3	30°C 25°C 20°C
	Level 5	3 4 5	3 3 5	2 3 4	2 3 4	2 3 4	1 2 3	1 1 3	1 1 2	30°C 25°C 20°C
	Level 5a	1 2 2	1 2 2	1 2 2	1 2 2	1 2 2	1 1 2	0.5 1 2	0.5 1 1	30°C 25°C 20°C
t>2.1mm TSOPs, SOICs <18 pins TQFPs or or TBGAs	Level 2a	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	28 ∞ ∞	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 3	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	11 14 20	7 10 13	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 4	∞ ∞ ∞	9 12 17	5 7 9	4 5 7	3 4 6	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 5	13 18 26	5 6 8	3 4 6	2 3 5	2 3 4	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 5a	3 5 6	2 3 4	1 2 3	1 2 2	1 2 2	1 1 2	1 1 2	0.5 1 1	30°C 25°C 20°C

608 610 606

FIG. 7
(Prior Art)

OIPE
MAY 1 9 2004
PATENT & TRADEMARK OFFICE
TC113

802

Package thickness	Level	Bake@125°C	Bake@40°c≤5%RH
≤1.4 mm	2a	4 hours	5 days
	3	7 hours	11 days
	4	9 hours	13 days
	5	10 hours	14 days
	5a	14 hours	19 days
≤2.0 mm	2a	18 hours	21 days
	3	24 hours	33 days
	4	31 hours	43 days
	5	37 hours	52 days
	5a	48 hours	68 days
≤4.0 mm	2a	48 hours	67 days
	3	48 hours	67 days
	4	48 hours	68 days
	5	48 hours	68 days
	5a	48 hours	68 days

Table 2 Reference Conditions for Drying Components that were Exposed to Conditions ≤60% RH (User Bake:Floor Life Begins Counting at Time=0 after bake)

FIG. 8
(Prior Art)

OIPE
MAY 19 2004
PATENT & TRADEMARK OFFICE

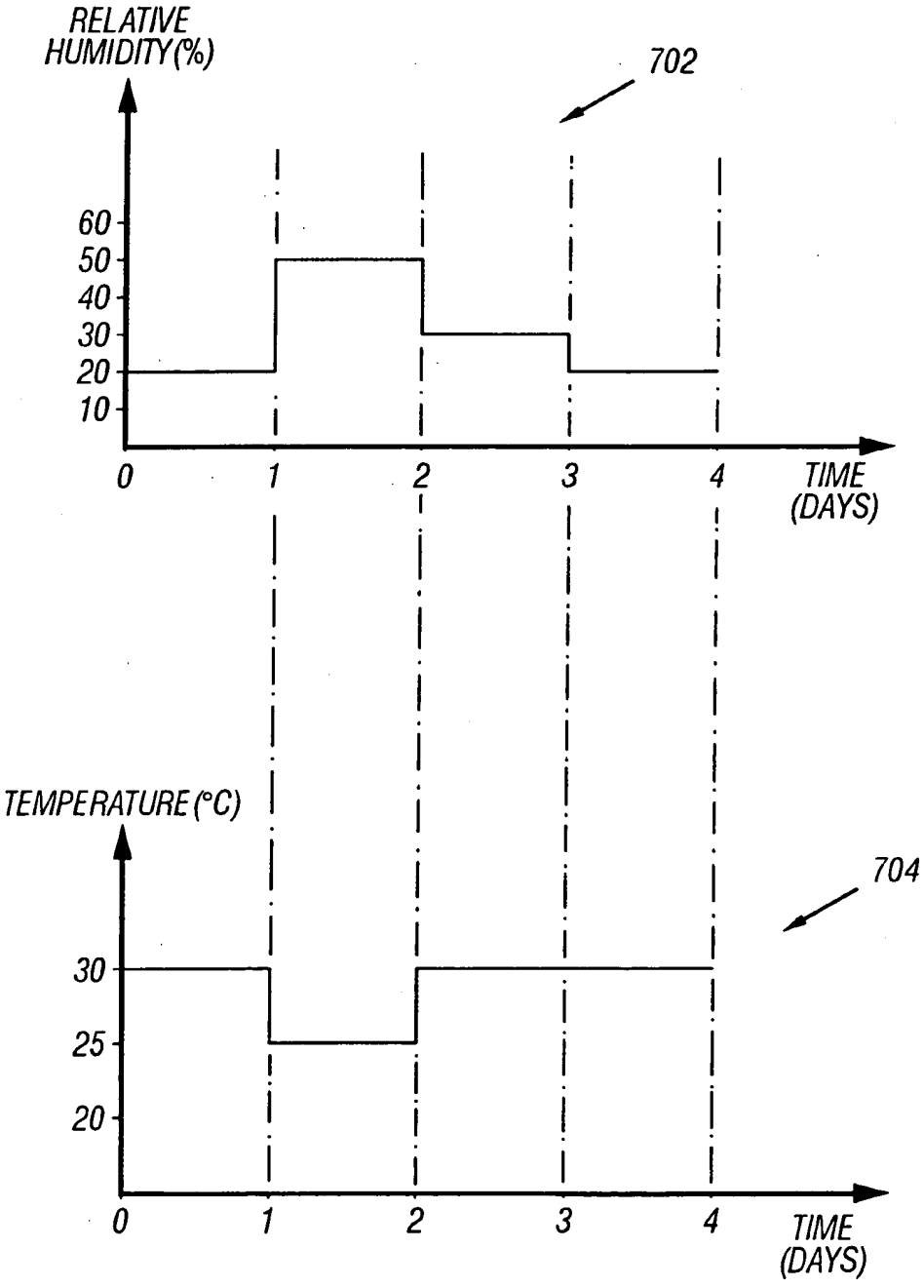

FIG. 9